

## EXECUTIVE SUMMARY

This White Paper will demonstrate both through empirical data and theoretical calculations, the cost and productivity impact that the silicon (both polysilicon and remelt) surface purity has on Cz ingot growth.

The pursuit of cost control, higher efficiencies and increased productivity are unrelenting efforts in all Cz growing operations world-wide. It is intuitively obvious that a higher initial charge density will allow a grower cycle to produce more kilos of ingot. The same is true of recharging and topping off operations. The goal is common and easily understood: More mass in equals more mass out equates to lower overall cost. What is not so obvious is the role played by the surface condition of the feedstock and particularly the small form factor material; it is the dominant characteristic in maximizing the gains of increased charge density. By using small feedstock with a surface purity of <5 ppbw (10-metal total) it is possible to realize a 10-13% gain in ingot yield when compared to only large size initial charge material and 3-5% when compared to lower purity small form factor material. The realized value of the higher charge density is greater with high purity material and more than offsets the additional cost.

It has been demonstrated conclusively that the use of price alone as a metric for the sourcing of silicon feedstock is at odds with the goals of cost reduction and increased productivity. The recent availability of high purity small form factor feedstock provides Cz growers with a new tool for improving bottom line economics.

## ABSTRACT

Crystalline silicon solar cells rely on high quality silicon to achieve greater levels of efficiency in converting sun light into usable power. Minority carrier lifetimes (MCL) are a key metric used to determine the quality of the crystalline silicon and MCL is heavily dependent upon the concentration of impurities and imperfections found in the bulk material. Using the Czochralski (Cz) pull method to grow single crystal silicon ingots, impurity concentrations vary predictably along the length of the ingot. In an orderly growth environment, one can predict the minority carrier lifetimes along the length of the ingot as a function of purity of the starting material. The Normal Freezing model for Cz silicon is used to quantify the impurity concentration profile within an ingot. The Shockley-Read-Hall model describing carrier recombination is then applied to predict minority carrier lifetimes for these ingots. Combining these two models, yield and

productivity levels of Cz silicon (single pull, batch recharge, and continuous) can be related to the purity of the silicon source material used to charge the crystal puller.

## INTRODUCTION

Crystalline silicon provides the most efficient commercially available solar cells. However, the most expensive element in the manufacturing of these cells is the silicon substrate. A tremendous amount of pressure is being exerted on the silicon supply chain, and in particular the ingot growth segment, to reduce costs. Cz growth companies have been reducing costs by purchasing lower quality source material, increasing charge size by incorporating small-sized fill material, using more reclaimed/recycled material, and extending growth cycles through batch recharge and continuous Cz. It is critical to understand how poly-silicon purity benefits each of these cost reduction efforts and the impact that “clean” source material can have on yield and productivity.

It is important to understand the role that the silicon substrate plays in solar cell efficiency in order to understand how source material (poly or recycled silicon) affects cell performance. When light strikes a solar cell, a negatively charge electron ( $e^-$ ) and a positively charge hole ( $p^+$ ) are liberated from the silicon lattice and free to move about the material. These charge carriers must then travel within the silicon wafer and reach the contacts of the solar cell in order to generate electricity. The efficiency of a solar cell is defined by how much electricity is generated when illuminated by the sun. Impurities in the silicon crystal act to annihilate these charge carriers before they reach the contacts and serve to reduce the efficiency of the solar cells. Solar cells are termed “Minority Carrier Devices” which means that current flow and hence power generation is dominated by electron flow ( $e^-$ ) in p-type solar cells and hole flow ( $p^+$ ) in n-type solar cells. We employ the term “minority carrier lifetime” or MCL to coincide with terminology used by cell manufacturers - high quality material has high MCL.

This paper describes the physics of impurity incorporation in silicon ingots grown using the Cz pull method and extends this to quantify its effect on minority carrier lifetimes. A simple mathematical formulation (that has been proven experimentally and accepted by the scientific community) is then introduced to demonstrate impurity segregation during Cz growth. This will be used to illustrate the impurity profile along the length of an ingot. At a similar level, a description of how these impurities degrade the minority carrier lifetime will also be presented.

Lastly, this paper relates the purity of the source material to yield and equipment productivity from the standpoint of minority carrier lifetime.

## IMPURITY SEGREGATION / NORMAL FREEZING MODEL

It has long been established that impurity incorporation in Cz silicon follows the Normal Freezing model. A brilliant detailed description can be found in Volume 1 of “Silicon

Processing for the VLSI Era” by S. Wolf and R.N. Tauber, Lattice Press<sup>1</sup>. The mathematical model is summarized here with a physical description to provide understanding. In the slowly changing environment of a silicon melt, one can assume the melt/solid interface remains near equilibrium and that impurities redistribute uniformly within the melt quickly compared to the solidification rate. Also one assumes that once the impurity is captured in the solid it is held in place and does not migrate appreciably or reincorporate into the melt. In the dilute melts typically encountered in silicon growth, the relationship between the concentrations of an impurities in the solid and the liquid can be described using the equilibrium segregation coefficient,  $k_o$ , as:

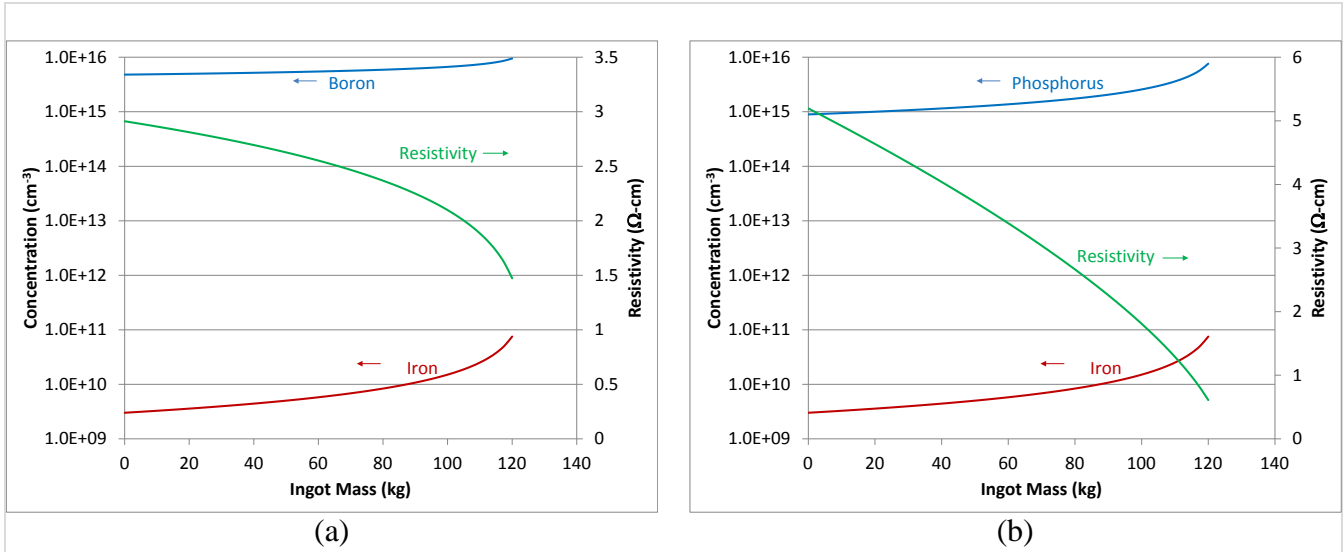
$$k_o = C_s / C_l \quad (1)$$

where  $C_s$  and  $C_l$  are the atomic concentrations in the solid (s) and liquid (l), respectively. (Note we are dealing with concentrations and not absolute numbers in this relationship.) Eq. 1 defines the balance between the impurity concentration in the liquid and the solid. For most relevant impurities,  $k_o$  is  $< 1$  (See Table I). Physically this means that the impurity concentration in the solid is less than that of the liquid, or the melt. Effectively the solid is rejecting impurities at the solid/melt interface – a naturally self-purifying process. If we assume that no impurities enter the system after the initial melt is established, the impurities reside either in the liquid or in the solid. Therefore in the case of standard Cz growth where the melt volume decreases faster than the impurity atoms incorporate into the solid,  $C_l$  continues to grow quickly – thus  $C_s$  increases to maintain the balance indicated by Eq. 1. This is the same model used to describe dopant incorporation for resistivity control and provides the mathematical understanding for what has been reduced to rule-of-thumb. Resistivity is higher at the top of an ingot than at the bottom. It is now easy to understand that small segregation coefficients lead to large concentration differences between the top of the ingot and the bottom.

Table I provides a list of common impurities used (in the case of resistivity control) or found in silicon. Figure 1 employs Eq 1. as a model depicting Cz growth for (a) p-type silicon and (b) n-type silicon where boron and phosphorus are used as dopants, respectively. At the same time we include a small amount of iron (Fe) as a contaminant in the melt. The plot illustrates how the dopant and iron (Fe) concentrations increase from the top of the ingot to the bottom. (Figure 1 also shows the resistivity profile in the ingot to calibrate the reader familiar with doped ingot growth.) Iron (Fe) was selected as the contaminant due to its relevance to minority carrier lifetimes and because as a constituent of stainless steel it is one of the most common lifetime killing contaminants found in crystalline silicon. Notice that the Fe concentrations are several orders of magnitude lower than boron – foreshadowing that small amounts of Fe have huge consequences.

**TABLE I.** Segregation Coefficients and Capture Cross Sections

Impurity	Al	As	B	P	Sb	C	Cu	Fe	Cr	Ni
$k_o$	0.002	0.3	0.8	0.35	0.023	0.00625	4E-4	8E-6	1.1e-5	1E-4
$\sigma_n$ (cm <sup>2</sup> )	--	--	--	--	--	--	2E-10	8E-14	4.1E-15	1.8e-16
$\sigma_p$ (cm <sup>2</sup> )	--	--	--	--	--	--	--	4E-15	9.1e-18	3.2e-17



**Figure 1.** Concentration profiles of (a) Boron and (b) Phosphorus and Iron in Cz grown ingot. The boron, phosphorus, and iron concentrations are calculated by using Eq. 1 in a system where the melt mass is decreasing as the ingot mass is increasing. The resistivity of the ingot is calculated from the dopant concentrations. Notice that the iron concentration is more than 5 orders of magnitude lower than the dopant concentration and that its value changes by 250% due to its much smaller segregation coefficient.

Understanding how material purity affects ingot quality is very important to the recycling loop. Recycling is required to drive silicon cost lower and the self-purifying nature of crystallization makes using recycled material very attractive. For the case of a 156 mm x 156 mm pseudo square cut from a 200 mm diameter ingot, approximately 24% of the ingot is cut off as slabs. From Figure 1, it can be seen that this material is excellent for recycling because the highest bulk impurity concentration at the bottom of the ingot is about 2 pptw (1E11 cm<sup>-3</sup>) which is 3 orders of magnitude better than semi-grade poly. To use this material effectively, one needs to resize it while maintaining the surface cleanliness.

#### MINORITY CARRIER LIFETIME

In the introduction, we described how solar cell efficiency depends upon the minority carrier lifetime (MCL). In the previous section we described how impurity atoms (Fe) incorporate in a silicon ingot and how the profile varies along the ingot's length. This section describes how the minority carrier lifetime is related to the number of impurity atoms in the silicon ingot and hence how the minority carrier profile can be predicted along its length. A rigorous description of this requires an understanding of semiconductor band theory which is well beyond the scope of this paper. However, a significant number of textbooks cover this material. A particularly good discussion can be found Volume VI of the Modular Series on Solid State Devices, "Advanced Semiconductor Fundamentals" by R.F. Pierret<sup>2</sup>. This subject is introduced to provide the reader with confidence that significant scientific work has been done to correlate impurity concentrations to minority carrier lifetimes and hence solar cell efficiency.

Band theory provides a means to describe how electrons are able to move through a semiconductor crystal. Band theory also serves to explain how different elements change the electrical properties of silicon - for instance how boron, an acceptor atom, creates a p-type material (or hole dominated resistivity) and phosphorus, a donor atom, creates electron dominated resistivity. The Shockley-Read-Hall (SRH) recombination-generation model describes how electron-hole pairs are created and annihilated using semiconductor band theory which is precisely the minority carrier lifetime.

Metal contaminants tend to reside deep within the energy gap and are referred to as trap levels. The term "trap" is used intentionally because holes or electrons are captured and effectively held in place until the opposite carrier (electron or hole) annihilates the pair whereby preventing the charges from reaching the device contacts. The effectiveness at which the metal atoms trap carriers depends upon where they reside in the energy gap. Using the SRH model and employing a few simplifying, yet valid, assumptions, the minority carrier lifetime ( $\tau_n$  or  $\tau_p$ ) can be described by a capture coefficient ( $c_n$  or  $c_p$ ) and the concentration of traps ( $N_T$ ) in the silicon:

$\tau_n = \frac{1}{c_n N_T}$	for p-type semiconductors	(2 a)
------------------------------	---------------------------	-------

$\tau_p = \frac{1}{c_p N_T}$	for n-type semiconductors	(2 b)
------------------------------	---------------------------	-------

where  $\tau_n$  and  $\tau_p$  are the electron and hole minority carrier lifetimes (units of seconds), respectively. (Note that electrons are minority carriers in p-type materials and holes are minority carriers in n-type materials.)  $c_n$  and  $c_p$  are the capture coefficients for minority carrier electrons and holes, respectively with units of  $\text{cm}^3/\text{sec}$  and  $N_T$  is the concentration of traps (metal atoms) in units of  $\text{atoms}/\text{cm}^3$ . ( $N_T$  will be replaced by  $C_s$  in Eq. 1.) The capture coefficients for holes and electrons can differ by more than an order of magnitude based upon the characteristics of the impurity. A more intuitive physical parameter used to describe the "size" of a "trap" is the capture cross section ( $\sigma$ ). This parameter has a more intuitive physical feel and therefore is favored in device literature when characterizing metal impurities. The capture cross section is related to the capture coefficient and is defined by:

$$c_n = \sigma_n v_{th} \quad (3 \text{ a})$$

and

$$c_p = \sigma_p v_{th} \quad (3 \text{ b})$$

where  $\sigma$  is the capture cross section (units of  $\text{cm}^2$ ) and  $v_{th}$  is the thermal velocity ( $\sqrt{\frac{3k_B T}{m}} \sim 10^7 \text{ cm/s}$  at room T). Experimentally, to determine the capture cross section of a metal contaminant, one introduces a controlled concentration of metal impurities (typically through ion implantation), then measures MCL using a time and temperature dependent pulsed conductivity method (Deep Level Transient Spectroscopy – DLTS), and by assuming random motion at the thermal velocity, Equations 2 and 3 determine  $\sigma$ .

Table I lists the capture cross sections for several common contaminants in silicon. Each impurity has two capture cross sections, one for minority carrier holes ( $\sigma_p$ ) and one for minority carrier electrons ( $\sigma_n$ ). Notice in Table I the large variation in values among the different elements as well as the differences in cross sections between holes and electrons. Also notice that  $\sigma_p$  is commonly much smaller than  $\sigma_n$ . This means that n-type semiconductors have an advantage in that their minority carrier (hole) lifetimes are longer than that of p-type materials – hence the higher efficiencies related to n-type solar cells. A few other notable items associated with capture cross sections are:

- (1) Larger cross sections reduce minority carrier lifetimes
- (2) Many metals have larger cross sections for minority carrier electrons
- (3) Iron (Fe) has a large cross section and is also one of the most common metal contaminants in Si due to the use of stainless steel in process equipment

## PURITY AND INGOT YIELD AND PRODUCTIVITY

We have shown in Figure 1 how the impurity concentration increases along the length of an ingot based upon the Normal Freezing model described by Eq. 1. Now using Eqs. 2 and 3, we can also quantify the minority carrier lifetime at any point in the ingot, and this is shown in Figure 2. Notice that the minority carrier lifetime is higher at the top of the ingot than it is at the bottom. Solar cell manufacturers require silicon wafers with carrier lifetimes above a minimum value in order to achieve a minimum cell efficiency. One can determine what portion of a silicon ingot meets or exceeds this minimum value by overlaying the MCL requirement on the MCL curve. This is a power tool for determining the effect of source silicon purity on ingot yield and equipment productivity.

In the introduction, we listed several ways in which ingot manufacturers are attempting to increase productivity:

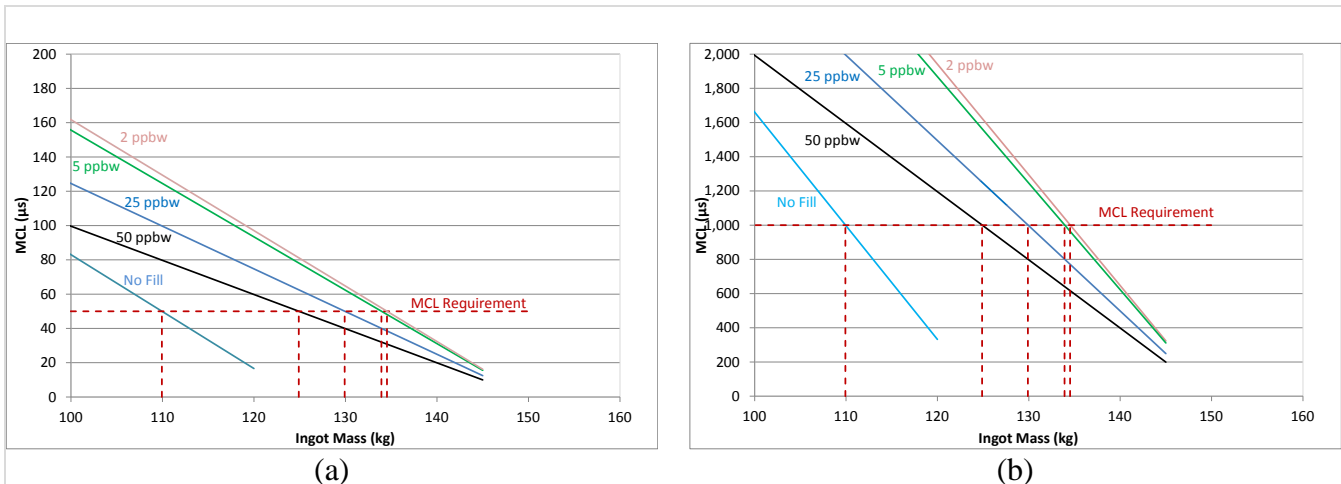
- (1) Increasing initial charge volume by filling gaps in the crucible with small size silicon
- (2) Increasing the use of reclaimed/recycled silicon

(3) Extending run length through batch recharge or continuous silicon feed.

Here we look at the effect on yield and productivity by increasing charge size from 125kg to 150kg in a standard Cz puller. The different scenarios for charge poly and the fill material are listed below in Table II. We assume the initial charge of 125kg is stacked and loaded into a Cz puller with an effective purity level of Fe of 15ppbw. Solar grade poly-silicon can meet this requirement, however, most impurities are introduced in the stacking and loading procedure and the penalty is assessed with every new load. Figure 2 illustrates the effect of increased charge size on the amount of material produced in a run. It also illustrates how high purity material increases both yield and productivity. Yield is calculated as the ratio of the mass of the silicon ingot that meets the minimum MCL ( $50\ \mu\text{s}$  for a p-type cell and  $1000\ \mu\text{s}$  for an n-type cell) to the mass of the initial charge plus the fill material. The productivity calculation is based upon a 24 x 7 operation of the tool where one run includes heat up, stabilization, growth, melt back, cool down and chamber turn. Productivity is estimated using the following conservative assumptions: average ingot solidification rate of 0.075 kg/min, a total run time of 72 hrs for a full-term ingot with a moderate dip ratio. It is believed the added fill material does not negatively affect the dip ratio and serves only to increase the growth time by about 5.5 hr. Using the 125 kg charge as a baseline process, the productivity increase is calculated as the increased silicon output produced in the slightly longer run time. (Note if the average run time for a baseline process is longer, the productivity increase will be even larger.)

**TABLE II.** Yield and Productivity Calculation for Increased Charge Size

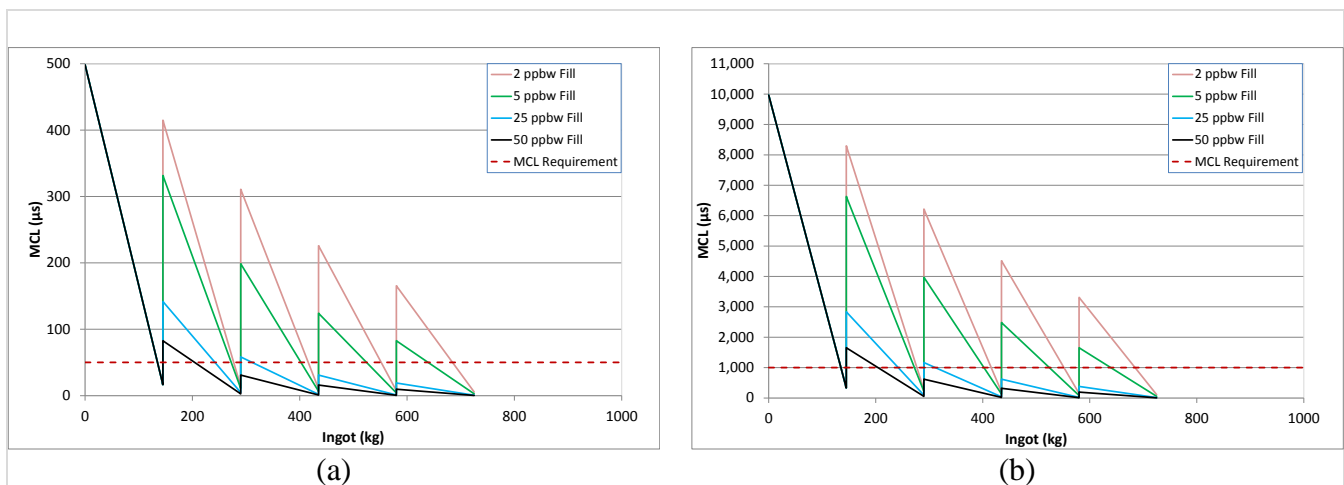
Scenario	CHARGE		FILL		INGOT Mass (kg)	YIELD Max (%)	PROD. INC (%)
	Amount (kg)	Purity (ppbw)	Amount (kg)	Purity (ppbw)			
1	125	15	0	--	110	88.0	--
2	125	15	25	2	134.5	89.6	13.6
3	125	15	25	5	134	89.3	13.2
4	125	15	25	25	130	86.7	10.0
5	125	15	25	50	125	83.3	5.6



**Figure 2.** Profile plot of the minority carrier lifetime of a CZ ingot (a) p-type and (b) n-type. The MCL requirements were selected such that the ingot mass is the same for both types of crystals. The No Fill ingot corresponds to a Cz ingot grown from a 125 kg charge with 15ppbw Fe. The other ingots were grown from 150 kg charge sizes where the first 125 kg contained 15ppbw Fe and the extra 25 kg contained 2, 5, 25, and 50 ppbw. Notice that the total quantity of silicon produced increases dramatically when the fill material is high quality. This leads to higher productivity for the crystal puller.

It is clear from Figure 2 and the data in Table II that increasing the initial charge with small size silicon, increases the puller productivity. However, the real increase comes when high purity fill material is used. While this is a very attractive proposal to increase yield and productivity, it is very common for fill material to be contaminated to levels much higher than 25 ppbw ( $6.3 \text{ E}14 \text{ cm}^{-3}$ ). This is because of the large surface area to volume ratio of the silicon. When sizing silicon for fill material, surface contamination becomes the dominant source of impurities because most resizing techniques involve the use of metal plates or crushers and these metals must be removed meticulously.

Similarly, we have calculated the effect of source material purity for batch recharge Cz. Batch recharge processes reduce the cost of some major consumables in the Cz system, in particular the quartz crucible. Batch recharge processes also has the advantage of eliminating heat up and cool down cycles since the crucible is left hot as the replacement material is inserted. Again, batch recharge processes require small size or flowable material which often requires active resizing of larger silicon. Figure 3 illustrates how silicon purity affects the amount of material that can be extracted in one cycle. Each spike in the Figure 3 corresponds to the beginning of an ingot. Each ingot is pulled until the proper amount of melt has been removed, and then the replacement material is introduced. For this calculation, we increased the flowable silicon contamination level from 2 ppbw to 50 ppbw to show that each successive ingot yields less material than its predecessor. It is easy to see that as the purity of the flowable material degrades, so does the amount of usable ingot. In the cases of 25 and 50 ppbw material, one yields less than two ingots.

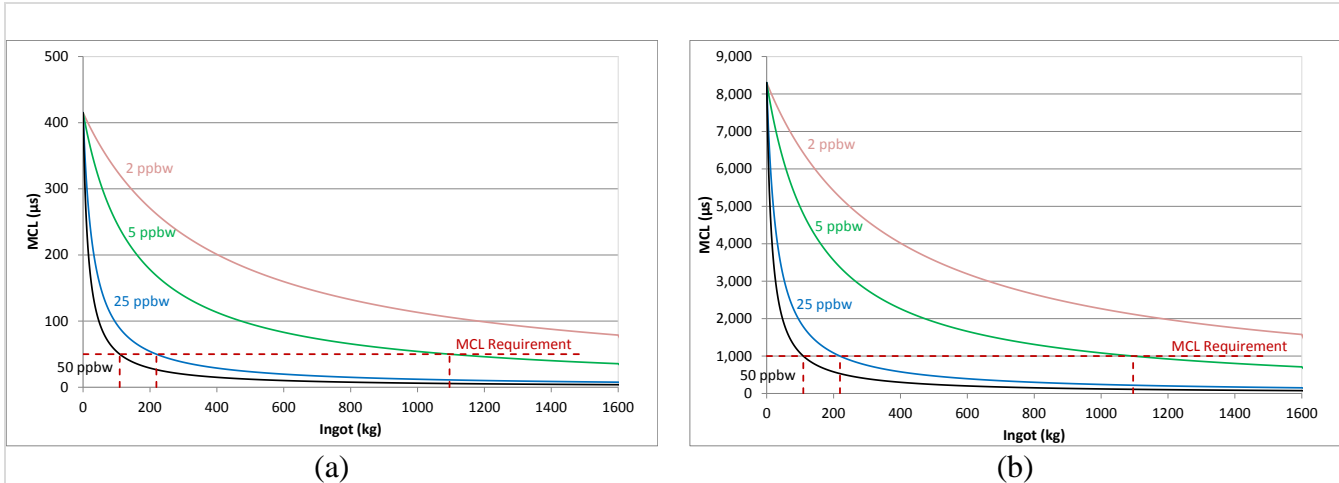


**Figure 3.** Profile of the minority carrier lifetime in silicon ingots grown using batch recharge Cz for (a)



p-type ingots and (b) n-type ingots. The MCL requirements were selected such that the ingot mass is the same for both types of crystals. Each “Spike” in the saw tooth corresponds to the start of an ingot. Notice that each successive ingot contains less material that meets the MCL requirement. Notice that only clean material allows a significant amount of silicon to be generated in one run.

Lastly, we apply the calculations to Continuous Cz (CCz). Continuous Cz has a major advantage over standard Cz and batch recharge Cz in that the impurity concentration in the melt increases much more slowly. This is because the melt level remains constant (and for the purpose of this illustration the melt mass is kept at 50 kg) because source material is being added at the same rate the ingot is solidifying. When this balance is achieved, a tremendous amount of silicon ingot can be removed from one run. If dopant material is added with the replacement silicon, one can achieve a constant doping profile in the ingot as well. Figure 3 illustrates the minority carrier profile for a CCz run. One sees a very strong dependence on the amount of ingot that can be extracted from a single run and the purity of the flowable material. Table III summarizes how much material can be extracted in a single run as a function of flowable material purity. If the flowable material purity is 5 ppbw or better, more than 1 metric done can be extracted from a single run.



**Figure 4.** Profile of the minority carrier lifetime in silicon ingots grown using continuous Cz (a) p-type ingots and (b) n-type ingots. The MCL requirements were selected such that the ingot mass is the same for both types of crystals. This assumes a melt mass of 50kg and the feed material is added at the same rate the ingot is grown. For extremely clean material (2 ppbw), the amount of high quality ingot grown is well over 1600kg. For flowable material containing 5 ppbw Fe, the ingot production exceeds 1 metric ton. Lower quality material severely limits the production of CCz material.

**TABLE III. Yield and Productivity for Continuous Cz**

Scenario	CHARGE		Flowable	INGOT
	Amount (kg)	Purity (ppbw)	Purity (ppbw)	Mass (kg)
1	50	15	--	
2	50	15	2	1600
3	50	15	5	1100
4	50	15	25	220
5	50	15	50	110

## SUMMARY

While the importance silicon purity has always been known, the effect on yield and productivity on Cz silicon has now been quantified. It is important to understand that cleanliness must be maintained throughout the silicon handling process especially when creating small sized silicon used for fill, recharge, and flowable processes. The information contained in Figure 2 and Table II illustrates the importance of fill material cleanliness on Cz productivity. Figure 3 extends that information to include the flowable material required for batch recharge. Figure 4 and Table III shows how dramatically the productivity of a CCz puller is affected by poor quality source material. In the arena defined by crystalline silicon solar cells where substrate cost plays a dominant role in yield and productivity, ingot manufacturers should revisit their silicon strategies and investigate how to maximize their productivity. Optimizing the use and purity of the small sized silicon can have a significant effect on the cost of creating silicon ingot.